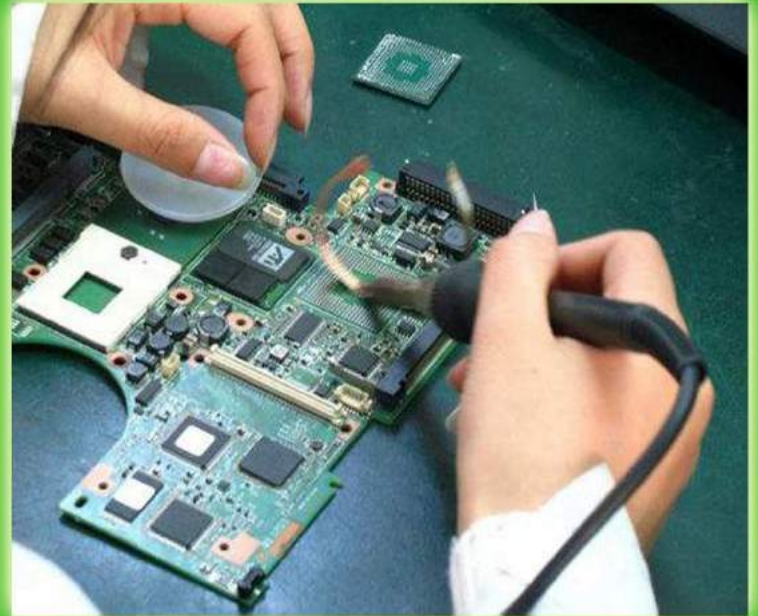
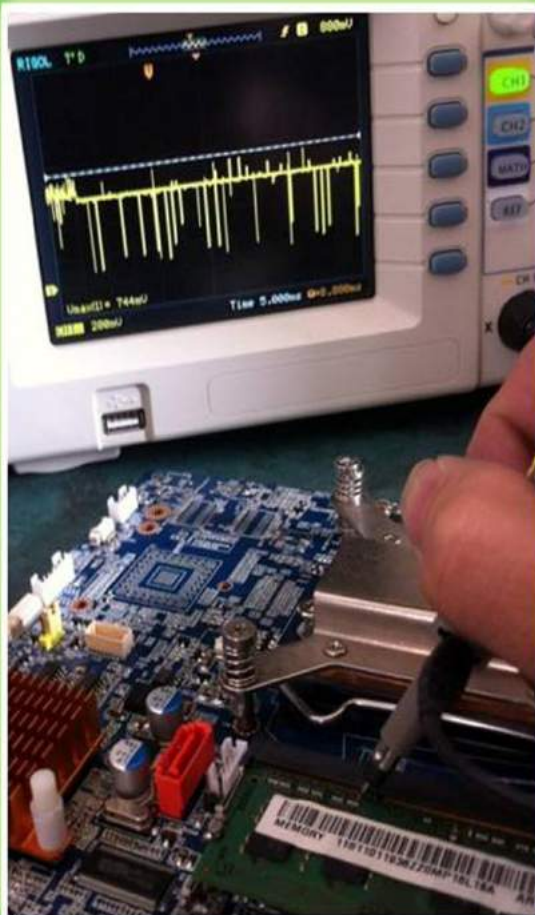


The Best of



Laptop Chip Level Repair Guide



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for signal level laptop level repair, you must know how to measure and analysis the signals of the mainboard. So the perfect laptop repair solution is: Components Level + Signal Level repair!

1.2: The Basic Knowledge You Must Know Before Starting to Repair Laptop

1) The basic electronic repair knowledge you must know:

- a) The analogue and digital circuits.
- b) What are the opened circuit, short circuit, leakage circuit and etc.
- c) For the laptop repairer, you must know what's the "signal" and "timing sequence".
 - I. **Signal** = When a laptop mainboard working, it will sends and receives different data and commands to control the circuits. So the signal is very important for a laptop mainboard to working properly.
 - II. **Timing Sequence** = The meaning of Timing Sequence is as the name of "Timing" and the "Sequence". When a laptop mainboard supply an AC to it, press power button until it start-up/opening successfully to working. At the same time mainboard each circuit will sends and receives the signals in between their correct timing and sequence, to successfully start-up/open the mainboard and ready to use by the user. The timing sequence is important, and must need to follow. If one of the step missing or incorrect timing, it will cause the mainboard not working. Even the markets have many brands laptop, but all or most of them are just using the Intel or AMD platform chipset only. So the same chipset is using the same timing sequence to work. And then we can just learn these two main chipset timing sequence, we can handle and repair the laptop easily.

Chapter 2

Original & OEM Laptop Mainboard Part Numbers

All branded laptop computer like Acer, Dell, HP, Lenovo and etc, they are not manufacture their laptop mainboard/motherboard. All of them are using the third party company design laptop mainboard to build their own brand laptop computer. This is because the branded computer company they want to earn more money and cut the cost to build a laptop computer.

The entire third party laptop computer mainboard manufacturer called it as an OEM company/manufacturer. What is the difference to OEM (Original Equipment Manufacturer) and ODM (Original Design Manufacturer) company? The OEM company is responsible to manufacture the product, but not include the product design and research. But the ODM company is do all these thing, so the branded computer company just put their brand name and model into this laptop as their new model of laptop computer. For example the ODM product manufacture by ECS G550 is using in different brands and models of laptop computer like TCL610, ChangCheng E2000, FangZheng T5800D and etc.

We can say most of the laptop computer company is using the OEM and ODM product to build their laptop computer now. All these OEM & ODM laptop production company are from Taiwan and their manufacturer base is in China. The popular OEM & ODM company like: Compal, QUANTA, Wistron, Inventec and Pegatron. These OEM company have a huge market percentage on production of laptop mainboard. The second line OEM manufacturer like: MITAC, Clevo, FIC, MSI, ECS, Flextronics, Foxconn, Topstar and etc.

In the laptop maintenance, we can see different brands and models of laptop computer send to repair. After dismantle the laptop and found it different brands and models of laptop, but they also use the same laptop mainboard. So their mainboard circuits, timing sequence and repairing steps also the same. We need to know how to identify the laptop mainboard part number and their OEM manufacturer by which company.

2.1: Quanta

QUANTA is one the top OEM laptop mainboard manufacturer. Their OEM laptop mainboard is using by big laptop computer company like: Dell, HP, Lenovo, Apple and etc.

The Quanta OEM laptop mainboard part number is starting from DA or DAO. Their part number is DA or DAO and in between MB with 3 digits or 4 digits. The Quanta mainboard p/n model CH3 is shown in figure 2-1. In this model of laptop mainboard schematic diagram, you can find the “PROJECT: CH3” on bottom right there, as shown in figure 2-2.



Figure 2-1: Quanta CH3 mainboard part number

Chapter 3

The Architecture of the Laptop Mainboard

Now the chipset used by the mainstream laptop on the market is only two manufacturers. The Intel and AMD Intel is the absolute dominance. Once the most popular nVIDIA has quit the chipset industry in 2010, on the market, the notebook computer products with nVIDIA chipset are few.

3.1: The Architecture of Intel Double Bridges (GM/PM45 and below)

The Intel Double Bridge architecture includes the 855-GM/PM45 chipset. In the Intel Double Bridge architecture, their CPU & North Bridge both are connected through the FSB (Front Side Bus) and the North Bridge also control the memory, PCI-E 16X discrete graphics card and display output interface.

The North Bridge and South Bridge bus connected is called as HUBLINK before. But it is renamed to DMI (Direct Media Interface) now and their transmission speed increased much faster.

The South Bridge is control peripheral extension interface, mainly in the following:

USB: Devices on the USB line are USB interface, camera, Bluetooth and etc.

Audio card: MODEM and the audio card are on the same line.

ZS/HK5 Chief River BLOCK DIAGRAM

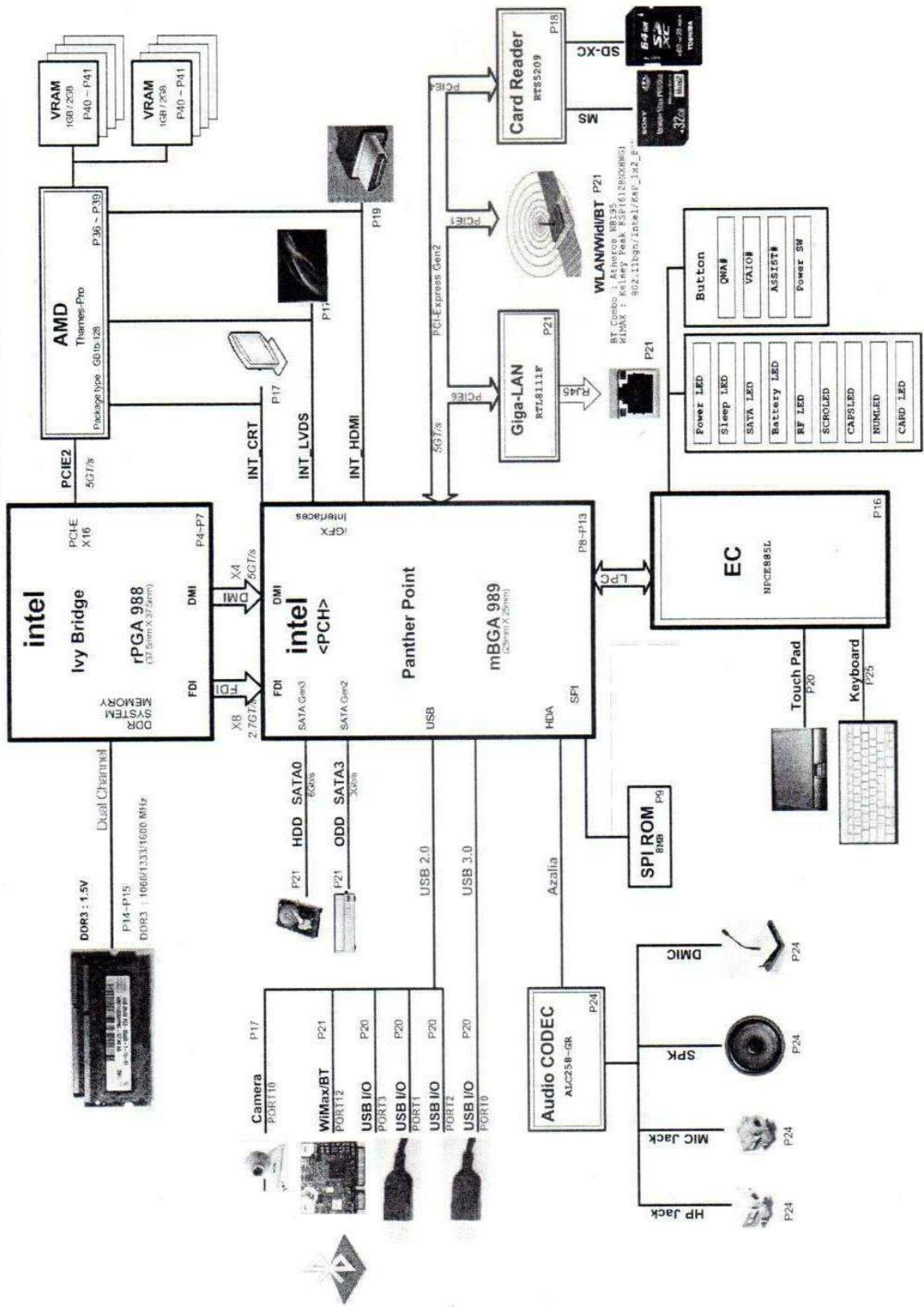


Figure 3-2: The architecture of Intel HM75 chipset

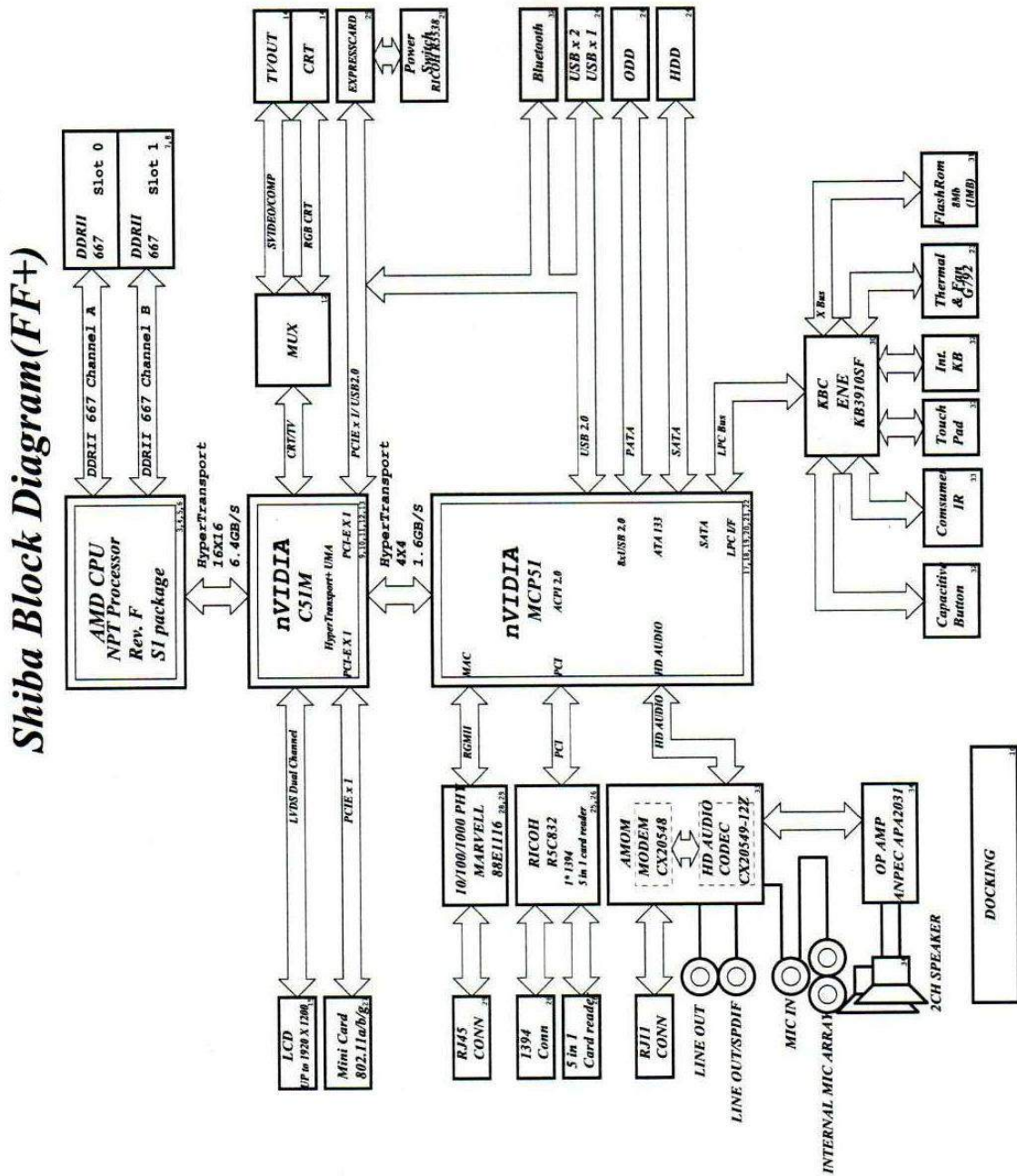


Figure 3-5: The architecture of nVIDIA C51M chipset

4.9.2 Quanta

Some of common signals names/symbols about Quanta Mainboard shown in table 4-2.

Signal Names/Symbols	Description
VIN	The common point voltage
ACIN, ACOK	Power Adapter detection
3V_AL, 5V_AL, VL	3V, 5V Linear power supply
+3VPCU, +5VPCU	EC Standby power supply
3V_S5	The voltage under the condition of S5; The South Bridge power supply; Opened by EC after Trigger switch.
+3VSUS, +5VSUS	The voltage under the condition of S3; Memory power supply; Sent by EC and opened by SUSON.
NBSWON#	Trigger signal for power on; Press the power on key to produce high-low- high signal to EC.
DNBSWON#	EC sent high-low-high effective trigger signal to the South Bridge PWRBTN#.
SLP_S3#, SLP_S4#	ACPI controller signal sent by the South Bridge is used to opening voltage when the power is turned on, and it also used to shutting off voltage when the power is turned off.
S5_ON	The opening signal of the South Bridge standby voltage sent by EC; Its use to convert the PCU to voltage S5.
SUSON	After EC receiving SLP_S5# from the South Bridge, then producing S3

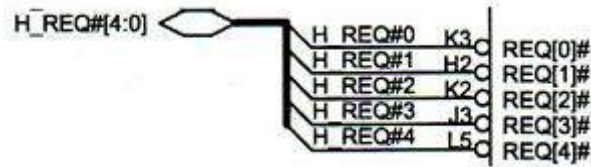


Figure 6-13: The similar signal circuit diagram

6.2: The Use of Common Point Bitmap (BoardView Software)

I. CASTW----*.1st

CASTW is the point position figure used by IBM, the most outstanding characteristics of this point position figure is that we can see the actual direction of signal. The red indicates that the signal is in the current layer, and the yellow indicates that the signal is in the other layer. Here "the other layer" refers to the other side of PCB and also refers to the middle layer of PCB. Here is the common use operations and shortcut menu shown in figure 6-14.

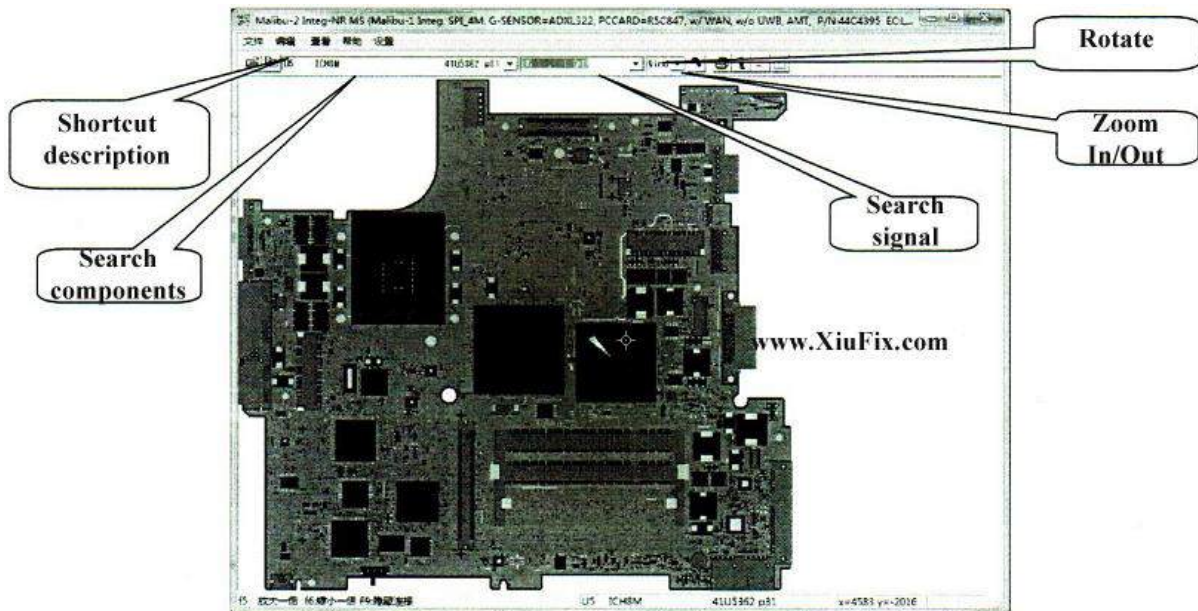


Figure 6-14: The screenshot of IBM BoardView software (point position figure)

Second, observe the architecture, in machines can be repaired on the current market, there are four kinds of connection ways for EC and BIOS, as shown in figure 7-3.

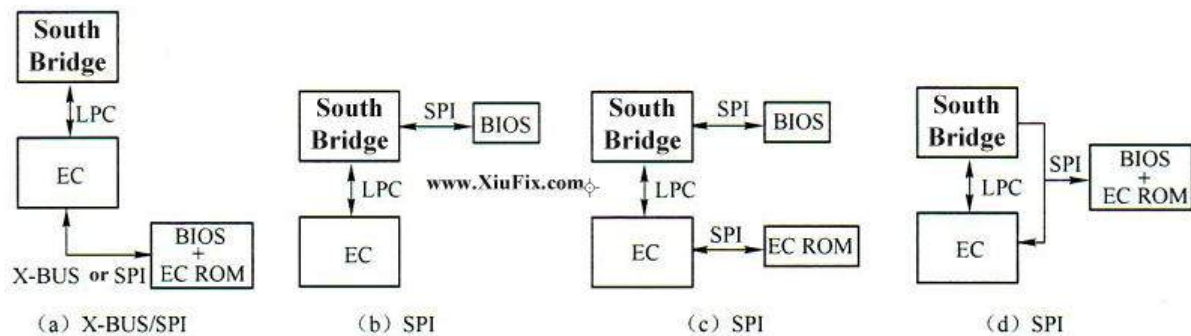


Figure 7-3: The relational graph of EC and BIOS

Firstly, BIOS connects to EC through X-BUS and SPI bus, and then EC connects to the South Bridge through LPC, in general, in this case, EC code is placed in the BIOS, that is share a chip with BIOS.

Secondly, BIOS connects to the South Bridge through SPI bus, there is not ROM under EC, it uses its own internal ROM. Common in ThinkPad and Apple, some models of the latest Lenovo also use this way.

Thirdly, the main BIOS connects to the South Bridge through SPI bus, hang a SPI ROM chip under EC for storing EC CODE, such EC is not comes with the program.

Fourthly, EC and the South Bridge connect BIOS through SPI bus, such EC is not comes with program.

7.2: The Function and Working Conditions of BIOS

BIOS is the program to provide the lowest level and the most direct hardware control in the computer system. It controls the input device and output device of the computer system, and is a hub connected the software program and hardware device. For the PC, BIOS includes the controlling keyboard, display screen, disk drive, serial communication device and some other functions of the code. The computer technology develops into today, there are all kinds of new technologies, many of the techniques of software part is to use BIOS to manage

Chapter 8

The Basic Working Process of Laptop Computer

As professional laptop computer maintenance, personnel, in addition to have a certain basic knowledge, also need to understand the working process and Intel chipset standard timing of the laptop and other maintenance theories knowledge. This chapter focuses on the boot process and Intel standard timing.

8.1: The General Boot Process of Laptop Computer

The working process of the laptop follows a certain sequence. In the repair of the laptop, in most cases, Timing applied on the power-on part in the system boot, so also called Power Sequence. Mainly refers to a laptop motherboard having done from standby to CPU get RESET signal. So literally, timing is time and sequence. The motherboard from standby to power-on, and then to CPU work, we feel just a short time. is almost a second, but in the work of the motherboard, it will happen a lot of things in a second, from the standby voltage producing. to press the switch, and to the motherboard received the switch signal, then to send out each working voltage. And the motherboard made so much action; it will strictly obey an established order, that is to say, in the process of these steps, if the first step isn't completed. Then the next step is not start. And there is a strict time requirement between each step, some will be accurate to a few milliseconds, for example, PWRGD Signal generation requires that each voltage stabilize about 5ms will be sent.

From the above introduction, we can see that the timing has very important significance for the normal working of a motherboard, the most common fault, such as no electricity, no boot and others, there have an important relationship with the timing. It can be said that if you master the timing, then you have a basic idea of maintenance for all kinds of faults of the laptop.

8.1.1 Hard starting process and Intel chipset standard timing

1. Hard starting process in general.

The boot process of the laptop with Intel chipset (below series 4) is as follows:

(a) Without any electrical equipment supply power (no battery and no power), through 3V button battery to produce VCCRTC to supply RTC circuit of the South bridge, to keep the operation of the internal time and save the CMOS information.

(b) After plugging in the battery or adapter, produce the common point.

(c) Then produce the EC standby power supply (usually linear voltage), after the standby power supply is normal, EC supply power to crystal oscillator to produce the EC standby clock, the standby power supply delay produce EC reset, EC reads the program configuration own pin(BIOS chip select waveform as shown in figure 8-1).

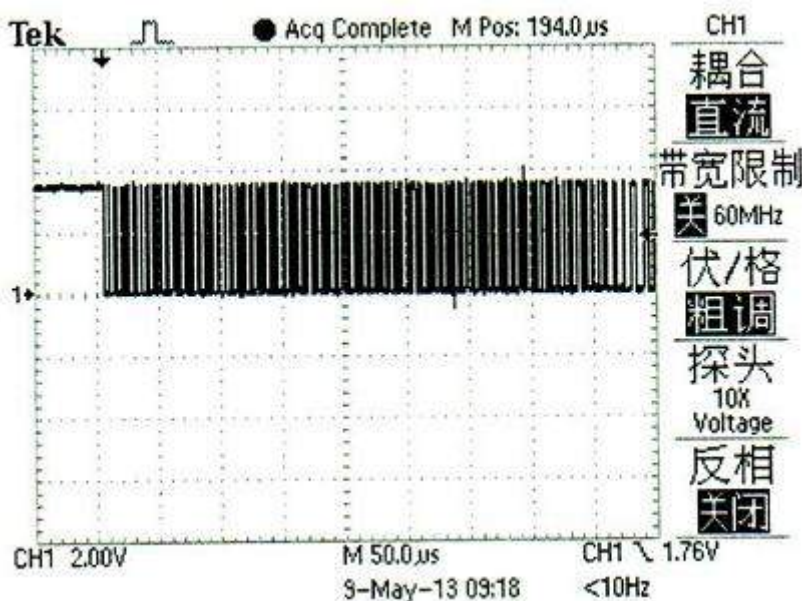


Figure 8-1: BIOS chip select waveform

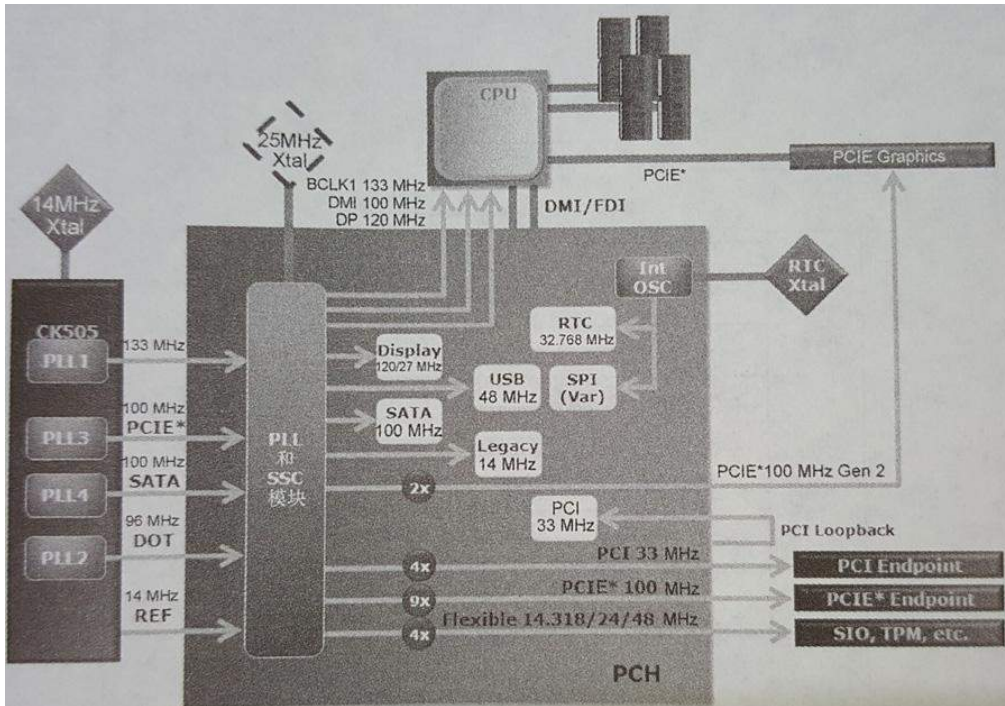


Figure 8-13

4. The clock signal distribution of above HM65 chipset

The clock signal distribution of above HM65 chipset is shown in figure 8-14, the characteristic is that it must be 25MHz crystal when the bridge integrates the clock chip.

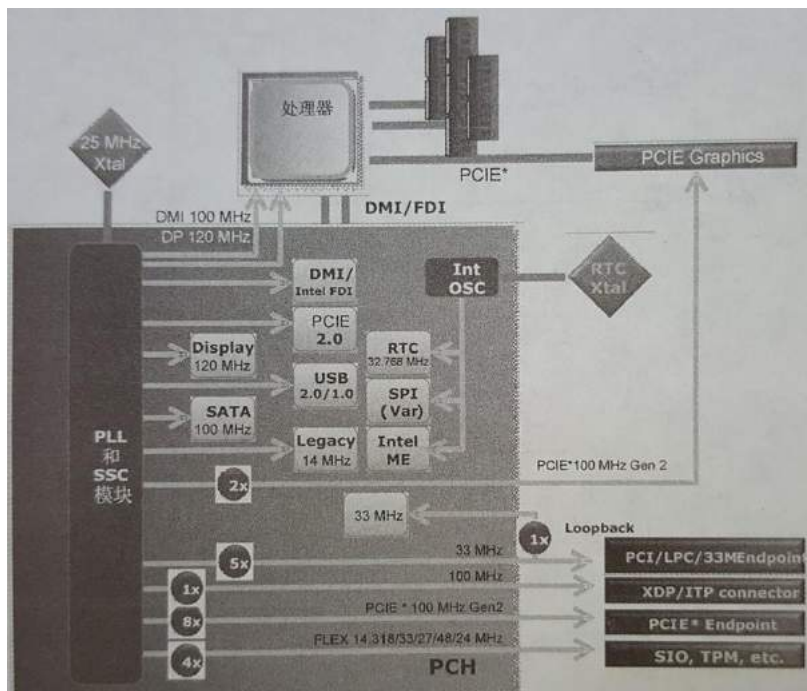


Figure 8-14: The clock signal distribution of above HM65 chipset

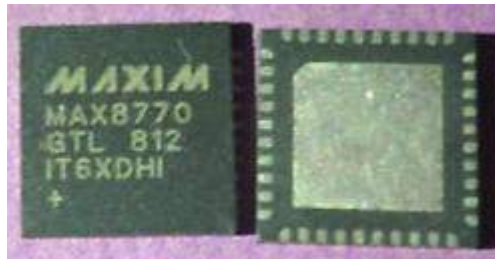


Figure 9-53: The real object of MAX8770

The definition of MAX8770 is shown in table 9-11.

Table 9-11: The pin definition of MAX8770

PIN	NAME	FUNCTION															
1	$\overline{\text{CLKEN}}$	Clock-Enable Logic Output. This inverted logic output indicates when the output voltage sensed at FB is in regulation. $\overline{\text{CLKEN}}$ is forced low during VID transitions. Except during startup, $\overline{\text{CLKEN}}$ is the inverse of PWRGD. See the <i>Startup Timing Diagram</i> (Figure 9). When in pulse-skipping mode (DPRSLPVR high), the upper $\overline{\text{CLKEN}}$ threshold is disabled.															
2	PWRGD	Open-Drain, Power-Good Output. After output-voltage transitions, except during power-up and power-down, if FB is in regulation then PWRGD is high impedance. During startup, PWRGD is held low and continues to be low while the part is in boot mode and until 5ms (typ) after $\overline{\text{CLKEN}}$ goes low. PWRGD is forced low in shutdown. PWRGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). When in pulse-skipping mode (DPRSLPVR high), the upper PWRGD threshold comparator is blanked. A pullup resistor on PWRGD causes additional finite shutdown current.															
3	$\overline{\text{PSI}}$	Logic Input to Indicate Power Usage. $\overline{\text{PSI}}$ and DPRSLPVR together determine the operating mode as shown in the truth table below. Blank the PWRGD upper threshold when the part is in skip mode. The part is forced into full-phase PWM mode during startup, while in boot mode, during the transition from boot mode to VID mode and during shutdown: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>DPRSLPVR</th> <th>$\overline{\text{PSI}}$</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>Very low current (1-phase skip)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Low current (approximately 3A) (1-phase skip)</td> </tr> <tr> <td>0</td> <td>0</td> <td>Intermediate power potential (1-phase PWM)</td> </tr> <tr> <td>0</td> <td>1</td> <td>Max power potential (2- or 1-phase PWM as configured at CSP2)</td> </tr> </tbody> </table>	DPRSLPVR	$\overline{\text{PSI}}$	Mode	1	0	Very low current (1-phase skip)	1	1	Low current (approximately 3A) (1-phase skip)	0	0	Intermediate power potential (1-phase PWM)	0	1	Max power potential (2- or 1-phase PWM as configured at CSP2)
DPRSLPVR	$\overline{\text{PSI}}$	Mode															
1	0	Very low current (1-phase skip)															
1	1	Low current (approximately 3A) (1-phase skip)															
0	0	Intermediate power potential (1-phase PWM)															
0	1	Max power potential (2- or 1-phase PWM as configured at CSP2)															
4	POUT	Power-Monitor Output: $V_{\text{POUT}} = K_{\text{PWR}} \times V(\text{CSNpm, GND}) \times \Sigma V(\text{CSP}_-, \text{CSN}_-)$, where K_{PWR} is the power monitor scale factor: $\text{CSNpm} = \text{CSN12}$ for MAX8771. $\text{CSNpm} = \text{CSN2}$ for MAX8770/MAX8772. POUT is zero in shutdown.															
5	$\overline{\text{VRHOT}}$	Open-Drain Output of Internal Comparator. $\overline{\text{VRHOT}}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{\text{VRHOT}}$ is high impedance in shutdown.															
6	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components such that the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.															
7	TIME	Slew-Rate Adjustment Pin. Connect a resistor R_{TIME} from TIME to GND to set the internal slew rate: $\text{Slew rate} = (12.5\text{mV}/\mu\text{s}) \times (71.5\text{k}\Omega / R_{\text{TIME}})$ where R_{TIME} is between 35.7k Ω and 178k Ω . This slew rate applies to transitions into and out of the low-power pulse-skipping modes (and to the transition from boot mode to VID mode. The slew rate for startup and shutdown is 1/8 this value. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the one set by R_{TIME} as defined above.															
8	TON	Switching-Frequency Setting Input. An external resistor between the input power source and TON sets the switching period ($T_{\text{SW}} = 1/f_{\text{SW}}$) per phase according to the following equation: $T_{\text{SW}} = C_{\text{TON}} (R_{\text{TON}} + 6.5\text{k}\Omega)$ where $C_{\text{TON}} = 16.26\text{pF}$. TON is high impedance in shutdown.															
9	CCV	Integrator Capacitor Connection. Connect a $470\text{pF} \times (2/\eta_{\text{TOTAL}}) \times 300\text{kHz}/f_{\text{SW}}$ capacitor from CCV to GND to set the integration time constant. The integrator is internally disabled when the part is in skip mode and the output is above regulation.															

0	1	1	1	-	s	0	0	0.750	1	1	1	1	1	0	0	0
0	1	1	1	1	1	0	1	0.737	1	1	1	1	1	0	1	0
0	1	1	1	1	1	1	0	0.725	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	0.712	1	1	1	1	1	1	1	0

The application circuit of MAX8770 is shown in figure 9-59, several key working conditions are indicated in the figure:

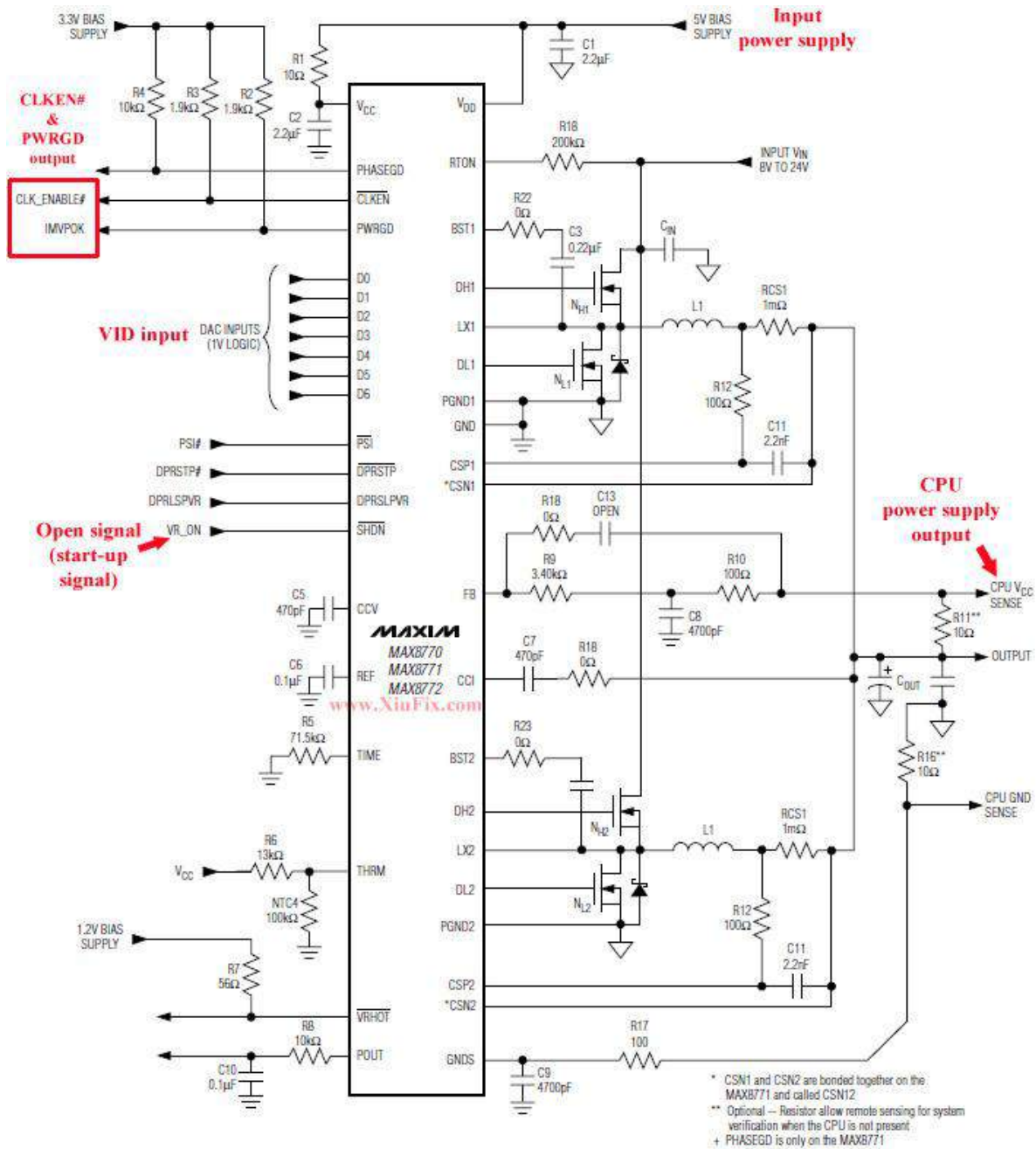


Figure 9-59: The typical application figure of MAX8770

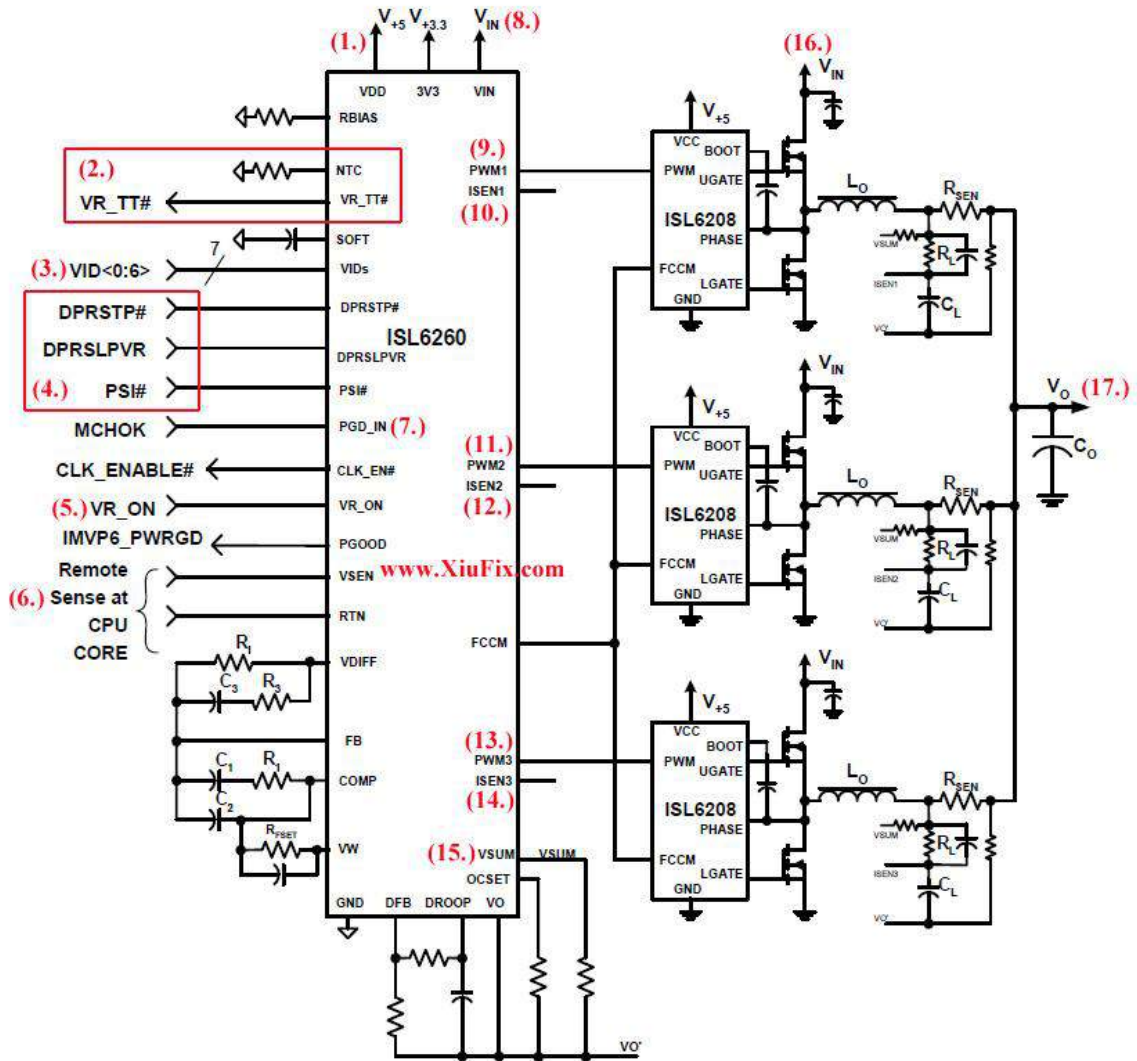


Figure 9-65: The simplified application diagram and the key pin of ISL6260

Note:

- (1.) = The chip main power supply
- (2.) = Temperature measurement and over-temperature instruction
- (3.) = VIDs
- (4.) = Sleep and Energy-saving control
- (5.) = Opening (start-up)
- (6.) = The voltage detection
- (7.) = The condition of PGOOD
- (8.) = CLK_EN# module power supply
- (9.) = First phase square waveform output

Chapter 12

Analysis of COMPAL OEM Laptop Mainboard Circuit

The greatest feature of the motherboard designed by Compal is the protective isolation and the standby circuit. the power-on sequence and the RTC circuit is almost the standard sequence. This chapter introduces three kinds of Compal protective isolation circuit. Then explain one of the Compal standby circuit.

12.1: Analysis of Compal LA-5891P Protective Isolation and The Standby Circuit

In this section, takes Compal LA_5891P as an example to analyze the protective isolation and the standby circuit.

1. The protective isolation circuit

Insert the adapter, through the power connects to PJPI, and produces VIN, 19V through PL24, is shown in figure 12-1. The figure of Compal motherboard power interface is shown in 12-2.

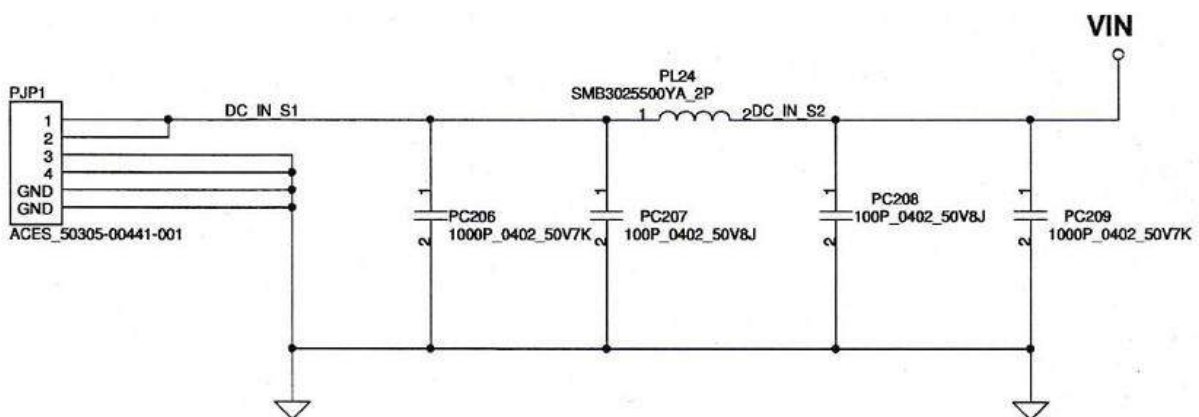


Figure 12-1: The production of VIN

Chapter 13

Analysis of INVENTEC OEM Laptop Mainboard Circuit

Inventec is usually OEM for HP. In this chapter, as DosXX Dunkel 1.0 (HP_6510b) an example to explain part of the circuit of Inventec, the circuit of this type is basically completed by the independent components, EC seldom participated in voltage control It is very meaningful for study of the circuit analysis.

13.1: Analysis of Inventec DosXX Dunkel 1.0 Protective Isolation Circuit

The voltage +VADP of the adapter interface JACK1 needs through Q507 and Q514 to reach the common point +VBATR, these two of field-effect tube is controlled by ADP_EN#, BATCAL#, ACDRV#, is shown in figure 13-1.

In the figure 13-1, Q507 is P channel. It must have two conditions to conduct: ADP_EN# is low, BATCAL# is high, and the origin of them is shown in figure 13-2.

The circuit analysis in the figure 13-2:

(1) LIMIT_SIGNAL is about 7V voltage from the adapter middle pin, +VADP is the adapter voltage 19V, through R108 and R105, R104 partial pressure, then

gets 5.9V of 2 pin, and less than 7V of 3 pin the comparator outputs the high level ADP_ID, then sends to EC for adapter detection.

(2) VADP through R108, R105 and R104 partial pressure to be 4.8V to send to 5 pin is less than 7V of 6 pin, the comparator outputs the low level ADP_EN#.

(3) The low level of ADP_EN# makes Q7 cut off, ADP_EN is high. sends to EC, because it's no power at this time, SLP_S3#_3R is low, Q545 is cut off, BATCAL# is pulled up to get the high level by the adapter voltage through R9252.

Then the Q507 is conducted successfully and produces +ADPBL.

In the figure 13-1, if Q514 is conducted completely, it needs the low level of ACDRV# sent by U5(BQ24703), the specific process is that +VADPBL in the left side of Q514 through the body diode between the D pole and S pole and D510 supplies the small current to the common point +VBATR, is shown in figure 13-3.

+VBATR renamed to be +VBATP after crossing the jumper wire PAD6, supplied to VIN of the standby power management chip TPS51120, as the main power supply. is shown in figure 13-4. Because EN3 and EN5 of the chip is hung in the air, according to the pin definition of TPS51120, EN3 & EN5 being hung in the air will produce automatically VREG3 and VREG5. VREG5 retraces to supply the power to V5FILT, and produces the reference voltage with 2VREF.

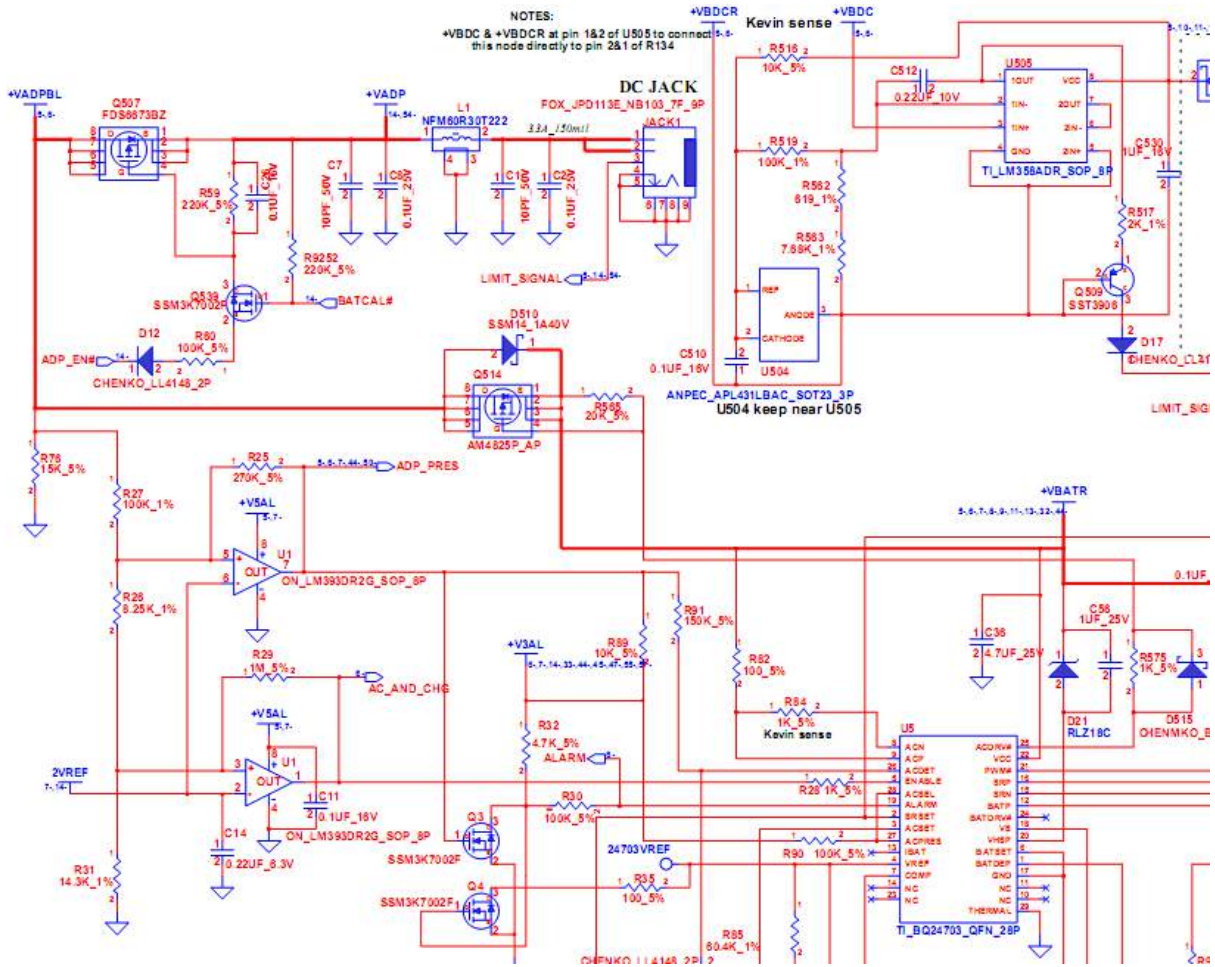


Figure 13-1: The common point production circuit

(For more clear details, please check their full schematic diagram on the bonus section)

Chapter 14

Analysis of Intel PCH Sequence (i3/i5/i7)

PCH is the platform controller hub. Intel PCH is the single bridge chipset in the Intel company. The product of the first generation PCH is Intel 5 series, such as Intel HM55 and so on. matches the first generation 13/15/17 CPU; the second generation and the third generation is Intel 6 and Intel 7 series, matches the second generation and the third generation 13/15/17 CPU, these two of generations is almost the same, CPU is in common used. The newest fourth generation has been released is Intel 8 series. PCH chip has all functions of the original ICH, also has the function of management the engine of the original MCH. It does not matter to call PCH the North Bridge or the South bridge. In this chapter, we mainly introduce the main feature of Intel 5 series.6 series and 7 series sequence.

14.1: About Intel ME and Intel AMT

Intel ME is the Intel Management Engine, is the independent hardware inset the North Bridge or PCH. ME firmware (ME FW) and the BIOS motherboard are usually kept in the same chip, but they are independent mutually. The architecture of Intel ME and ME firmware is shown in figure 14-1.

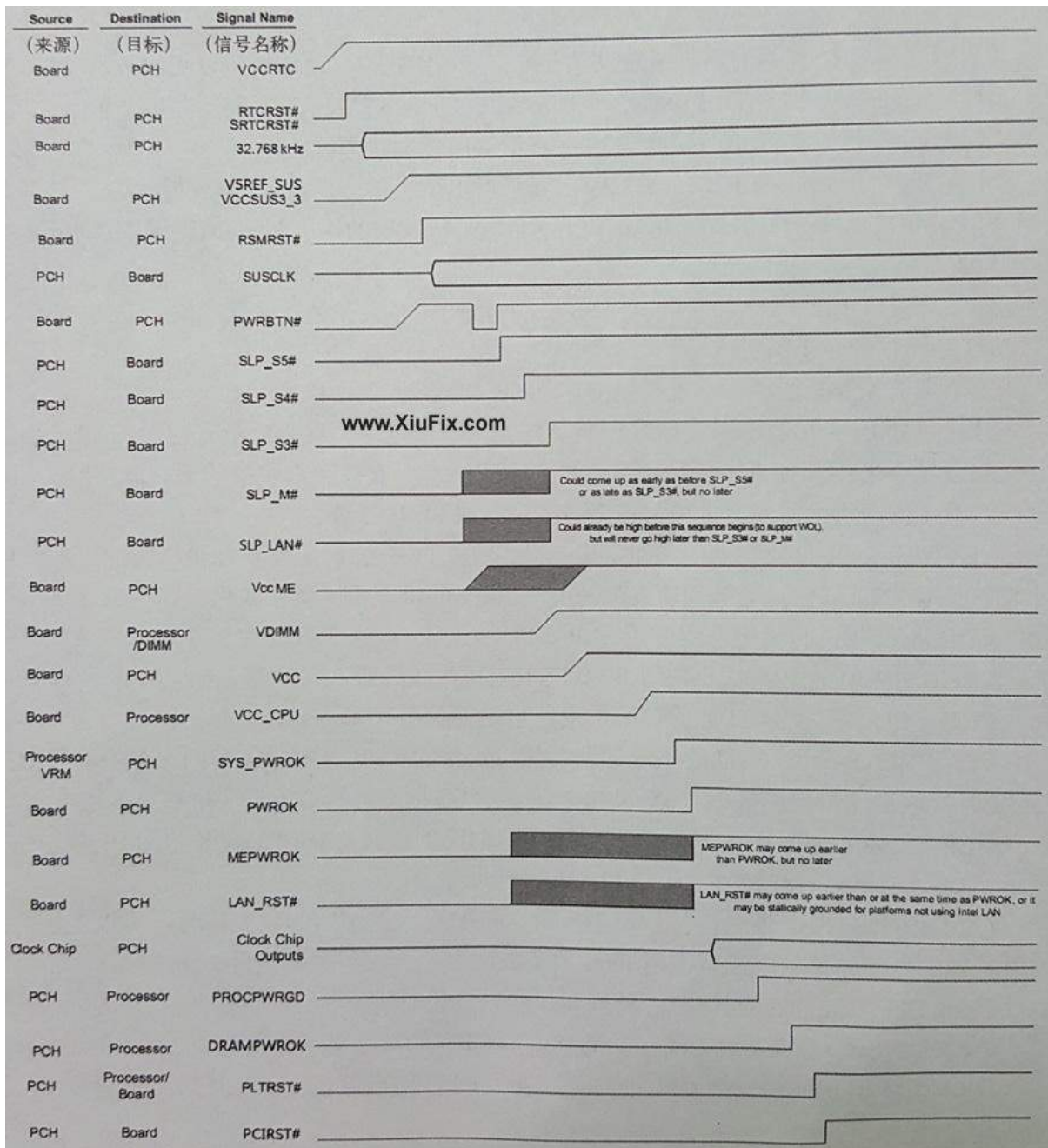


Figure 14-10: The timing sequence of Intel 5 series chipset

VCCRTC: 3V power supply sent from the motherboard to PCH Bridge, supplies the power to RTC circuit of the bridge, to save the CMOS parameter.

RTCRST#/SRTCST#: 3V high level sent from the mainboard to the bridge, the reset signal of RTC circuit start from ICH9, there have two resets.

32.768kHz: the 32.768 kHz crystal next to the bridge, the bridge supplies the power to the crystal, and the crystal supplies the frequency to the bridge.

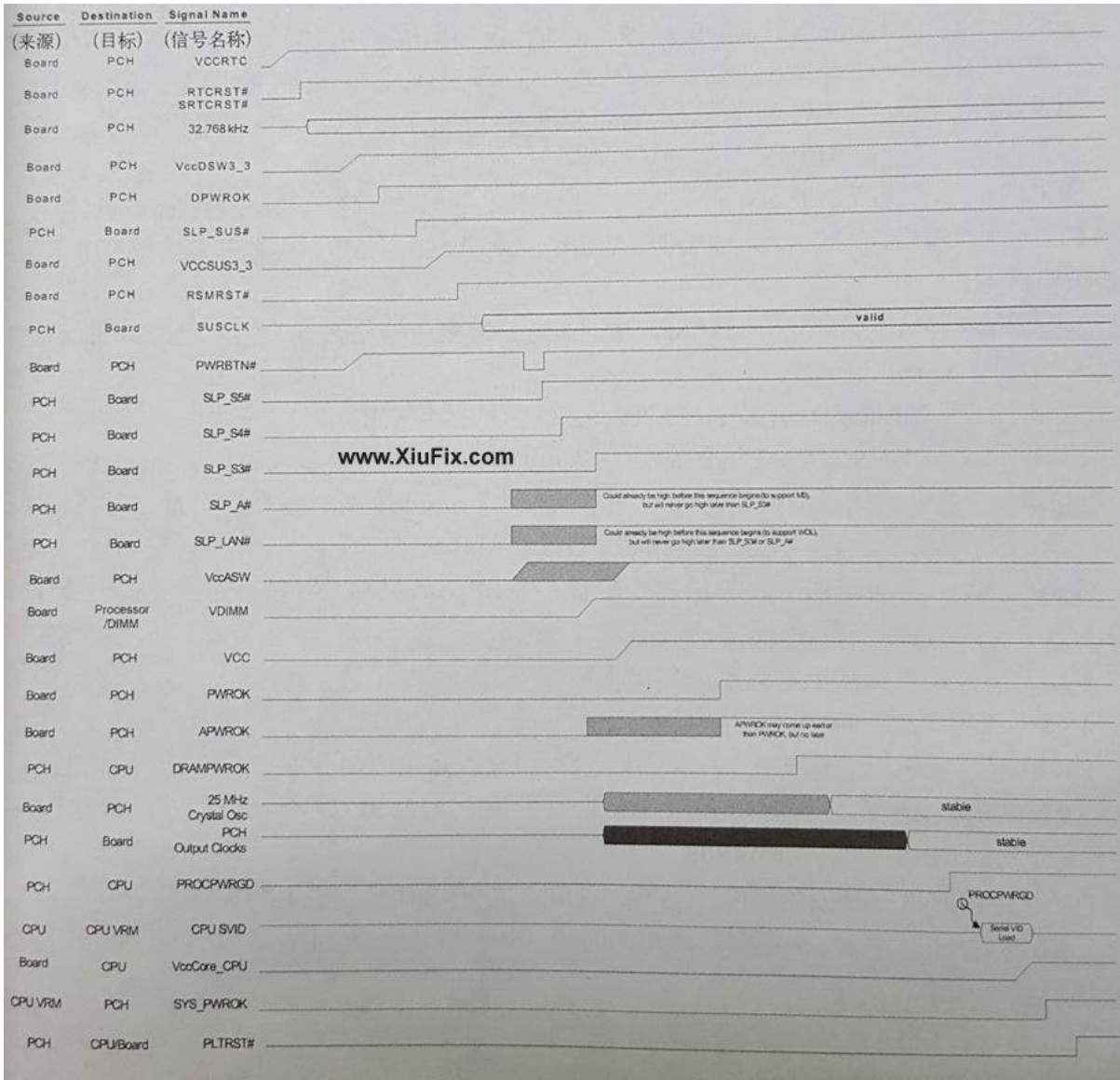


Figure 14-11: The timing sequence of Intel 6 series chipset

VCCRTC: sent 3V power supply to PCH bridge from the motherboard, supplies the power to RTC of the bridge, to save CMOS parameter.

RTCRST#/SRTCST#: sent 3V high level to the bridge from the motherboard, the reset signal of RTC circuit. Start from ICH9 and there have two resets.

32.768kHz: 32.768 kHz crystal next to the bridge, the bridge supplies the power to the crystal, and the crystal provides the frequency to the bridge.

VCCDSW3_3: the motherboard provides the deep sleep well power supply to the bridge, 3-3V. When it not supports the deep sleep, this voltage connects with VCCSUS3_3.

Chapter 15

Analysis of ASUS K42JR (HM5x) Timing Sequence

ASUS K42JR uses Intel 5 series chipset. We will analyze the standby and the power-on timing sequence under the adapter mode, because RTC circuit is almost the same, so we do not explain in this chapter.

15.1: The Standby State

First, the adapter insert, outputs A/D_DOCK_IN, is shown in figure 15-1.

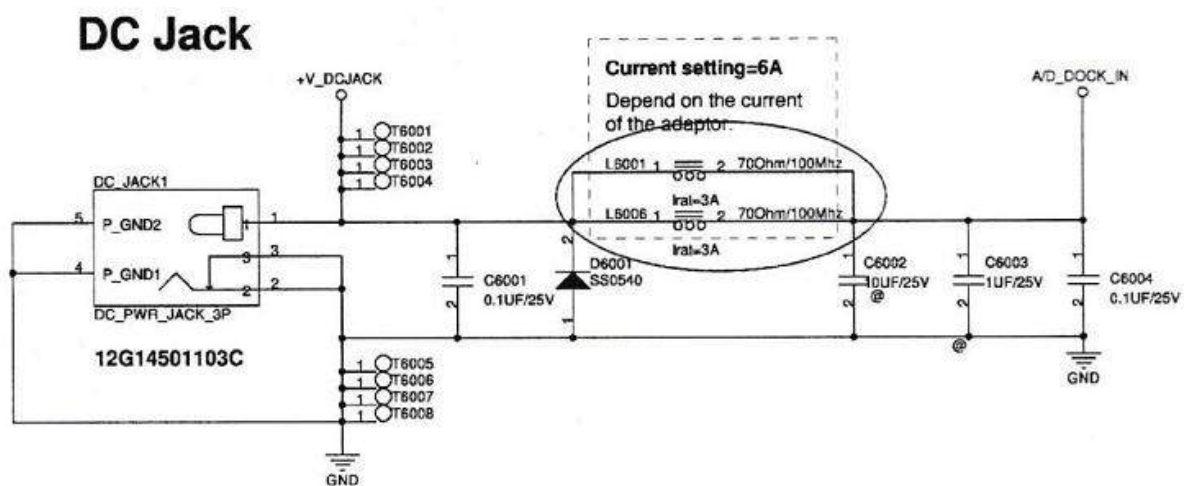


Figure 15-1: The screenshot of the adapter interface circuit

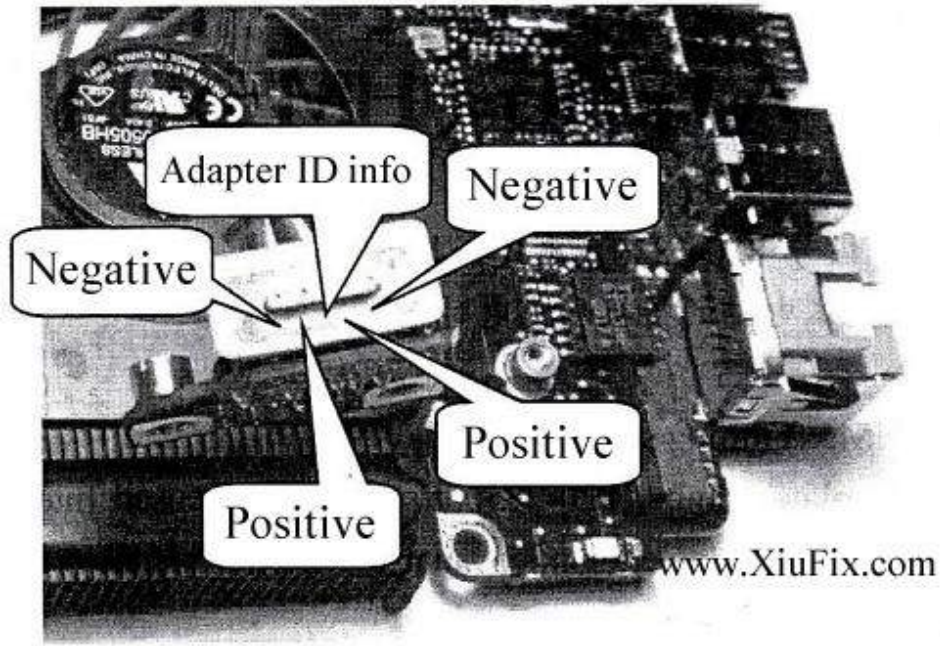


Figure 16-2: The kind of the Apple adapter

PPDCIN_G3H through the body diode of Q7080 to produce PPDCIN_G3H_OR_PBUS is shown in figure 16-3. (In the battery mode, the battery through the body diode of Q7055 and through the top tube Q7030 of the charging circuit, then through the body diode of Q7085D to supply the power to PPDCIN_G3H_OR_PBUS).

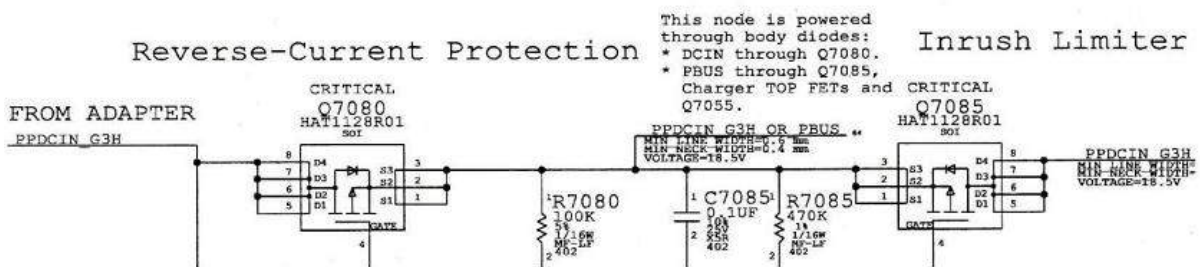


Figure 16-3: The production circuit of PPDCIN_G3H_OR_PBUS

PPDCIN_G3H_OR_PBUS supplies the power to VIN of U6990 (IT3970), and is added to EN directly, the chip outputs PP3V42_G3H, is shown in figure 16-4. This is a step-down switching regulator, internal integrates the booster and the clamping diodes. The pin definition VIN means the power supply, EN means the open, and RT means the oscillation setting. BOOST means start boot-strap pin, SW means phase/output pin. FB means feedback, BD connects the internal boost diode and the voltage regulator.

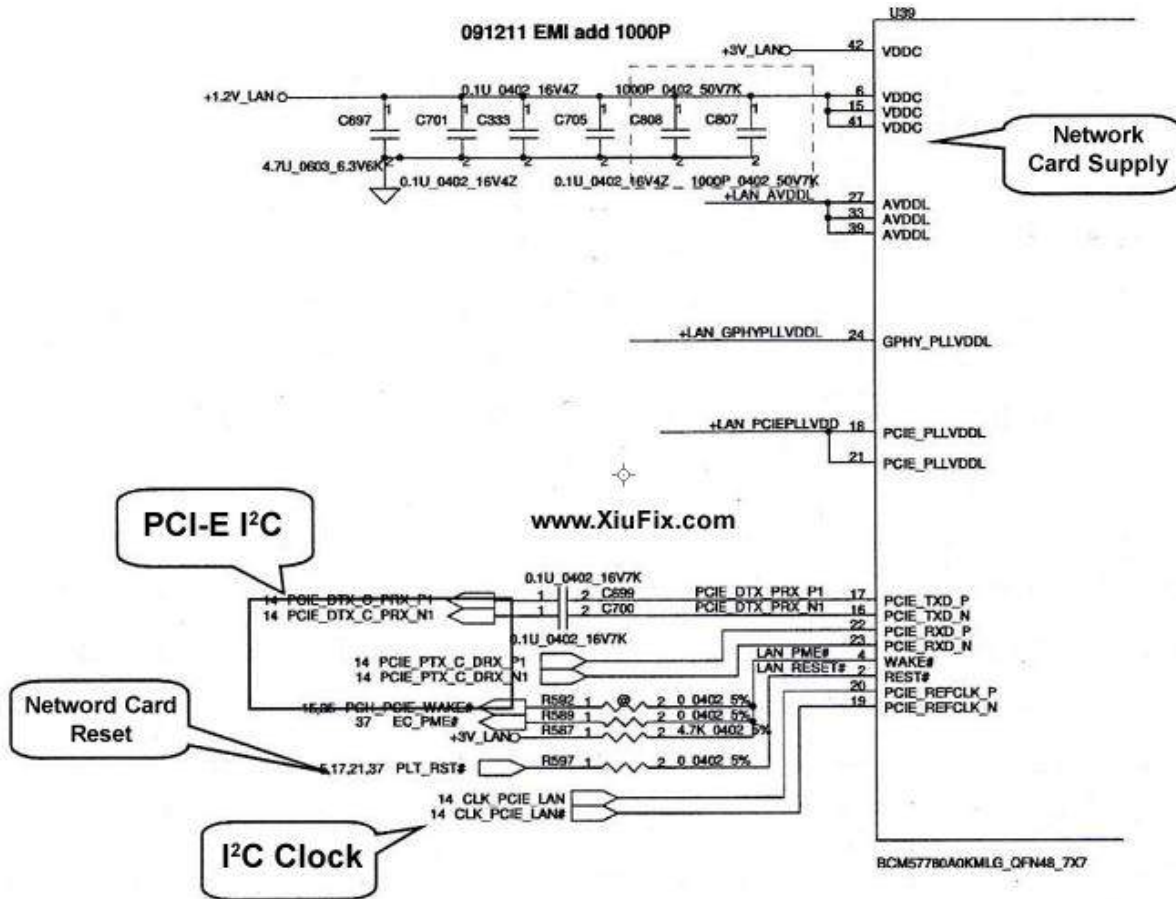


Figure 21-41: The screenshot of the basic working condition of the network card

(2) The crystal 25MHz of the network card, is shown in figure 21-42.

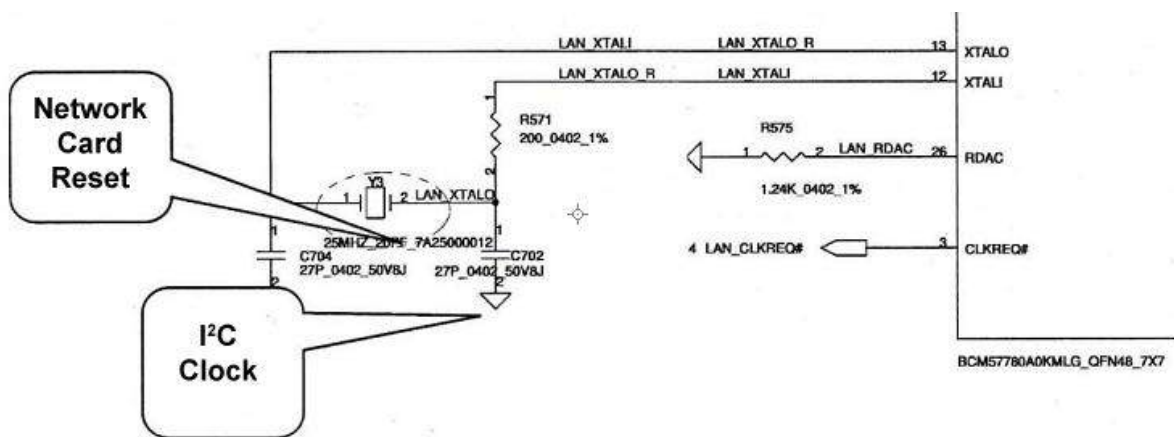


Figure 21-42: 25MHz crystal of the network card

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